Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.125”**

**ANODE**

**.105”**

**Top Material: Al**

**Backside Material: TiNiAg**

**Bond Pad Size: .099 X .099” min.**

**Backside Potential: CATHODE**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .105” X .125” DATE: 10/4/22**

**MFG: INT’L RECTIFIER THICKNESS .014” P/N: 16CYQ100C**

**DG 10.1.2**

#### Rev B, 7/19/02